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UDE 4.7 from PLS enables comprehensive control of up to six TriCore cores from a single user interface

Optimized Debug, Test, and System Analysis Tool for Infineon's New AURIX™ TC3xx Multi-Core MCU Family

Lauta (Germany), October 26, 2016 – By introducing version 4.7 of its Universal Debug Engine (UDE) at this year's electronica trade show (hall A6, booth A16), PLS Programmierbare Logik & Systeme presents an optimized debug, test, and system analysis tool that fully supports the internal debug functionalities of Infineon's new AURIX™ TC3xx multi-core microcontroller family without any limitation.

The multi-core SoCs of the second AURIX™ generation were specifically designed for electric and/or autonomous vehicles. Among other features, they offer a 300% increase in processing power compared to current high-end automotive microcontrollers. The MCUs included in the scalable AURIX™ TC3xx family can be equipped with up to 16 Mbytes of embedded Flash memory, more than 6 Mbytes of RAM and up to six 32-bit TriCore™ processor cores that operate independently. An additional lockstep core is included in four of the six TriCore cores supporting clock frequencies up to 300MHz, resulting in up to 2,400 DMIPS of processing performance for systems providing the highest safety assurance level (ASIL-D). Additional features of the TC3xx family include a radar processing unit with up to two Signal-Processing Units and a Hardware Security Module (HSM) encompassing asymmetric cryptography mechanisms meeting the requirements of EVITA 'high'. For use as host controllers in gateway and telematics applications, the devices also support a Gigabit Ethernet interface, up to 12 CAN FD channels according to ISO 11898-1 and a maximum of 24 LIN channels.

To let designers utilize this enormous complexity and performance in practical applications, UDE 4.7 as a true multi-core debugger enables controlling all TriCore™ processor cores from one single user interface. Depending on individual requirements, the cores can be controlled together, in groups or individually by traditional run-mode debugging, i. e. using breakpoints or single-stepping. In this mode, UDE enables all cores to be started and stopped almost synchronously using the devices' on-chip debug logic. Debugging complex applications is further simplified by multi-core breakpoints that can be used in shared code. A multi-core breakpoint will work all the time, regardless of which core is processing the code. Individually configurable views within UDE 4.7 additionally provide a better overview of multi-core applications.

Work is also made easier by the multiple options offered by UDE 4.7 for clearly visualizing system states at runtime, ranging from displaying application variables in memory to visualizing system parameters in diagrams.

For comprehensive system-level analyses and to ensure functional safety, UDE 4.7 additionally provides trace-based tools leveraging the AURIX™ TC3xx family's Multi-Core Debug System (MCDS). MCDS is exclusively available in the so-called Emulation Devices (ED) of the TC39xx family. For instance, these tools can be used to trace code execution for post-mortem analyses or to provide profiling information for run-time optimizations. In addition, UDE 4.7 provides the necessary code coverage to prove adequate test coverage.

Tight coupling of third-party test tools to the UDE and comprehensive scripting are enabled by the high-performance automation interface of UDE 4.7, which is based on Microsoft®'s Common Object Model (COM). As a unique feature, UDE is also independent of any proprietary scripting languages.

Communication with AURIX™ TC39xx microcontrollers is based on the two Universal Access Devices (UAD2pro and UAD3+). Suitable adapters are available for the JTAG interface and Infineon's proprietary DAP interface, with optional galvanic isolation for challenging environmental conditions. While UAD2pro exclusively uses the on-chip trace memory for MCDS tracing, large amounts of trace data can be read from the chip at up to 22.5Gbps using the UAD3+'s AURORA interface for storage within the UAD3+ and subsequent processing and analysis by UDE 4.7. Up to 4 Gbytes of memory are available within UAD3+ for this purpose.

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PLS Programmierbare Logik & Systeme GmbH

PLS Programierbare Logik & Systeme GmbH, based in Lauta, Germany, was founded in 1990. Since then, with its innovative test and development tools, the company has demonstrated its position as an international technology leader in the field of debuggers, emulators and trace solutions for embedded systems. The modular and flexible software architecture of PLS's Universal Debug Engine (UDE) guarantees optimal conditions for debugging SoC-based systems. For example, with the intelligent use of modern on-chip debug and trace units, valuable functions such as profiling and code coverage are available for system optimization and test. PLS's Universal Access Device product family (UAD2/UAD3+) complete the full featured debug solution with an efficient and high-speed target access with transfer rates of up to 3.5 MBytes/s and a flexible adapter concept supporting a wide range of different target interfaces. The leading edge UDE/UAD debugging infrastructure offers entirely new dimensions for fast and flexible access to multi-core systems with the support of important architectures such as AURIX/TriCore, Power Architecture, Cortex/ARM, XC2000/XE166 as well as simulation platforms of different vendors. For further information about the company, please visit www.pls mc.com.

For media-related inquiries, please contact:

PLS Programmierbare Logik & Systeme GmbH
Jens Braunes
Technologiepark
02991 Lauta, Germany
Phone +49 35722 384-0
Fax +49 35722 384-69
Email jens.braunes@pls-mc.com
Internet www.pls-mc.com

3W Media & Marketing Consulting
Werner W. Wiesmeier
Preisingerlohweg 2
85368 Moosburg/Aich, Germany
Phone +49 8761 759203
Fax +49 8761 759201
Email werner.wiesmeier@3wconsulting.de