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Technology Brief
RedHawk-3DX
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RedHawk-3DX:
Meeting Emerging Needs for Next-Generation 3D-IC and Sub-20nm Designs

To remain competitive in today's semiconductor market, integrated circuit (IC) designers need to meet ***performance***, ***power*** and ***price*** targets for their design, irrespective of its end application. Achieving these often mutually conflicting goals requires the use of several architectural and design techniques. Three-dimensional (3D) or stacked-die architectures can help meet performance and power targets by extending the integration capabilities beyond traditional system-on-chip (SoC) methodologies. The evolution of various low-power design techniques such as MTCMOS, voltage islands, and DVFS over the last decade, along with more recent design trends toward the use of sub-1V supply voltage levels, can help address stringent power requirements. On-die voltage regulators (LDO) are commonly being used to minimize the impact of package/PCB noise at these reduced voltage levels, enabling designers to maintain the robust supply voltage necessary to meet the devices' aggressive performance goals. To successfully reduce power, increase signal bandwidth and manage cost, it is essential to simultaneously optimize across the chip, the package, and board. As chips migrate to sub-20 nanometer (nm) process nodes and use stacked-die technologies, the ability to model and accurately predict the power/ground noise and its impact on ICs is critical for the success of advanced low-power designs and associated systems.

Reduced Supply Voltages

Reduced supply voltages in the sub-1V range are currently the norm rather than the exception. However, *increased functionality* (more logic per square micron area), *higher operating speeds* (3GHz+), and *cost focus* (less expensive package/PCB) has resulted in higher levels of noise in the design. This is not an optimal situation for devices already operating at reduced supply voltage levels because noise significantly degrades device performance, especially for cells in timing critical paths or clock tree networks. Accurate modeling of the power/ground noise is important for predicting the final operating voltage and the final operating speeds of the device and its accompanying system.

To ensure accurate modeling and simulation of the power/ground noise requires the following:

a) Extraction of the on-chip, package and PCB parasitics (inductance, capacitance and resistance)
b) Determination of the chip's various operating modes and transitions in a 'dynamic manner' (as compared to the 'static mode' in which all devices draw current during the simulation)
c) Consideration of through silicon vias (TSVs), interposer, and micro-bumps relevant to 3D/2.5D design modeling and simulation
d) Ability to simulate all of the above in time-domain, considering the chip (with its switching logic), the LDO and the package/PCB parasitics (primarily inductance)

RedHawk-3DX Technology

The release of Apache Design's fourth-generation power sign-off solution, RedHawk™-3DX, extends the capabilities of previous generations (SD (2003), EV (2006) and NX (2009)) to address sub-20nm designs with 3+GHZ clock speed and billions of gates to deliver significant improvements in full-chip dynamic power accuracy, capacity, coverage, and usability. It is architected to support the simulation of multi-die 3D-ICs, an emerging chip and packaging technology for low-power mobile, high-performance computing, consumer, and automotive electronic products.

For more than a decade, RedHawk has been the industry standard for solving critical power integrity issues and is used as a sign-off solution by the world's top 20 semiconductor companies. RedHawk's full-chip time-domain (and DC) simulation capabilities, VectorLess™ algorithm, and ability to enable both package-aware IC simulation and chip-aware package/PCB simulations, are production-proven over thousands of chip designs. Using the Apache Power Library (APL™) and proprietary modeling and simulation technologies, RedHawk has already enabled several generations of process technology migrations.

Advanced Simulation and Modeling

To ensure the performance of next-generation ICs, engineers need greater accuracy in their power noise simulation and a more comprehensive understanding of power behavior scenarios. Accuracy in dynamic voltage drop analysis is key for designs with significantly reduced noise margins caused by the lowering of supply voltages. RedHawk addresses these accuracy concerns with its well-proven capabilities including APL, on-chip inductance modeling, and support for multi-port broadband S-parameter package/PCB netlists. RedHawk-3DX advances the focus on accuracy with an emphasis in two areas: (1) sub-20nm extraction and EM modeling; and (2) sign-off coverage.

To address the growing complexity of power delivery network (PDN) design for sub-20nm nodes, RedHawk-3DX supports advanced process technology parameters and enables accurate extraction and modeling of the on-chip PDN parasitics (RLC). It also delivers advanced electro-migration (EM) checks that are current direction-aware, metal topology-aware, and temperature-aware. RedHawk-3DX supports strict sub-20nm manufacturing design rules for power and signal EM checks. These checks can be extended for current density checks associated electrostatic discharge (ESD) simulations using PathFinder™.

RedHawk-3DX improves the accuracy and coverage of dynamic power analysis by providing enhanced logic handling capabilities. Its new event- and state-propagation technologies with vector-based and VectorLess modes utilize both the functional stimulus and statistical probabilities to determine the switching scenario of the design.

The fast event-propagation engine enables an 'RTL2Gates' methodology by supporting the use of register transfer language (RTL)-level stimulus for dynamic voltage drop analysis. By using RTL VCD, designers can perform simulations without requiring the availability of the gate-level vectors. The RTL Power Model (RPM™) technology identifies the critical cycles in the RTL VCD (peak power or peak di/dt), that is

thenused by the RedHawk-3DX logic engine to determine the switching state of the complete design to perform cycle accurate dynamic voltage drop analysis.

The new state-propagation engine tackles the problem of 'toggle die-down' associated with most activity-based propagation engines. It uses toggle activity at the primary I/Os, register outputs, etc. as input to the state-propagation engine, which in turn uses proprietary '*smart detection* and *pruning'* techniques to eliminate the traditional problem of underestimating toggle rates in the logic cone. RedHawk uses the predicted toggle rates to perform time-domain VectorLess analysis, thereby bypassing the need for actual input stimulus.

RedHawk-3DX also supports a flexible mixed-excitation mode, in which some blocks use RTL or gate-level vectors (VCDs) while the rest of the design uses VectorLess to derive the chip's switching activity. This allows designers perform accurate full-chip dynamic power noise simulations by mixing simulation engines based on the availability of the stimulus.

Sign-off Capacity and Accuracy

It is well understood that power noise analysis is a global or '*full-chip'* problem. Unlike timing or cross-talk analysis it cannot be partitioned, because the noise or current flow in one part of the design may significantly affect another part of the design, due to shared PDN routing on the chip or in the package. So full-chip capacity, along with package/PCB model inclusion, is very important for the accuracy of final simulation results.

RedHawk-3DX provides hierarchical power grid (PDN) parasitic extraction and modeling technologies to deliver full-chip capacity and performance benefits, without sacrificing sign-off accuracy. Based on runtime performance and design analysis requirements, designers can perform hierarchical chip-level simulation using a model representation of all or most of their blocks and IP. The hierarchical model of the block captures its electrical signature and PDN parasitics in a compact format to help predict the block's impact on full-chip design and IC package without the cost of including the details.

Additionally, RedHawk-3DX's re-architected transient analysis engine provides considerable speed-up for every stage of the analysis including pre-processing, simulation and result post-processing. This speed-up benefit is especially seen in low-power ramp-up analysis where typically long simulation cycles are necessary to capture the power transient effects.

The use of on-chip LDOs is now becoming main-stream as they provide a more robust power supply for noise-sensitive parts of the design. However, LDO design must consider several factors:

a) Maintain robust output voltage for all operating scenarios
b) Supply the required current for all operating modes
c) Prevent the transfer of package/PCB noise onto the chip (and vice-versa)

Simulation of a design using an LDO not only requires complete modeling of the chip and its associated logic and power grid elements, but also necessitates an accurate behavioral modeling of the LDO circuit. This model should capture all the key operating behavior of the LDO, including the change in its output supply voltage for different load current scenarios. RedHawk-3DX's expanded low-power design simulation capabilities enable the creation and use of a behavioral model of the LDO circuit in full-chip power noise analysis. By using this model in full-chip static and dynamic simulations, it can predict scenarios of high drop at the LDO output due to excessive or fast current draw, or from line regulation issues caused by noise on the package/PCB traces that connect the on-board power supply (VRM) to the LDO input.

3D-IC and Stacked-Die Designs

Emerging chip and packaging technologies for stacked-die, 3D-IC architecture help reduce IC power consumption while enabling higher levels of integration. As designs migrate to stacked-die structures by employing silicon interposer and TSVs, RedHawk-3DX provides native support for simulating 3D-IC power noise and reliability issues. Designers can analyze their 3D/2.5D designs in two ways: concurrent mode, which simulates full layout details for all the chips including the interposer; or in model-based mode, which uses a Chip Power Model (CPM™) to capture the electrical signature (current and parasitics) for some chips whose layout may not be available. The flexible simulation environment of RedHawk-3DX allows design teams to explore various design configurations, which is important for early prototyping and planning of these complex structures.

For 3D-IC designs, RedHawk-3DX introduces a new multi-tab, multi-pane graphical user interface (GUI) that enables greater flexibility and productivity for analyzing multi-die designs. It provides the ability to simultaneously view DvD/IR hotspots and other results from multiple chips in a 3D/2.5D stack-up. It also offers multiple views of different results or layout images of a single chip simulation in the same display setting. This highly versatile innovative user environment, in conjunction with RedHawk Explorer, enables designers to qualify the input data, review overall design weaknesses, debug specific hotspots, and provide feedback to help develop more robust advanced chip designs.

Summary

In order to remain competitive in the semiconductor market today, chip designers must adopt an accurate and comprehensive chip-package-system analysis environment that uses a full-chip time-domain simulation. The new release of RedHawk-3DX extends previous generations' award-winning capabilities to sub-20nm process nodes and enables the simulation of 3GHZ+ designs with billions of gates. It is architected to support the simulation of multi-die designs to meet next-generation ***power***, ***performance,*** and ***price*** goals.

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