



PRESS RELEASE pls02-2015-E

Offers developers the ability to make full use of device-specific test and debug functions:

PLS' Universal Debug Engine 4.4.3 simplifies testing and debugging highly complex Xilinx Zynq-7000 SoC devices

Lauta (Germany), April 29, 2015 – PLS Programmierbare Logik & Systeme presents Version 4.4.3 of its Universal Debug Engine (UDE), which provides an optimized testing and debugging environment especially for the Xilinx Zynq-7000 SoC family of devices.

The All Programmable SoCs of the Xilinx Zynq-7000 family of devices combine for the first time dual-core ARM® Cortex™-A9 architecture with the functionality of complex Field Programmable Gate Arrays (FPGAs) on a single chip. In order to simplify development of appropriate powerful multi-core software, the UDE 4.4.3, among other things, enables users a flexible control of both cores within a consistent user interface. The cores can also be synchronously started and stopped, independently from each other or by grouping together in a so-called run control group.

Furthermore, the full support of all trace function units included on the SoCs ensures an especially efficient hard/software co-debugging. The UDE 4.4.3 support includes internal Program Trace Macrocell (PTM) for fast program trace in an on-chip memory as well as Coresight™ Instrumentation Trace Macrocell (ITM) that is important for troubleshooting and program measurements. A special Fabric Trace Macrocell (FTM) has also been integrated on the Zynq-7000 SoC devices for the output of internal signals from the FPGA logic into the common trace data stream. This unit, which simplifies debugging of the complex overall system, can also be configured by the UDE. Additionally, with PLS' Universal Access Device 3+ (UAD3+), a powerful hardware tool with 4 GB memory is available for recording external trace data. Besides trace, the debugger also enables very precise program runtime measurements by using the performance counter integrated on the SoC.

The system typically starts using a boot loader mechanism from an external flash memory. This can be programmed via the debugger. Connection of the UDE 4.4.3 with the Zynq-7000 SoC is achieved via JTAG. A digitally isolated connection to the target is also optionally possible with the Universal Access





Device (UAD) family. Furthermore, a full Eclipse integration with complete cross-debugger functionality is included in the UDE 4.4.3.

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PLS Programmierbare Logik & Systeme GmbH

PLS Programierbare Logik & Systeme GmbH, based in Lauta, Germany, was founded in 1990. With its innovative modular test and development tools, the company has demonstrated for over two decades its position as an international technology leader in the field of debuggers, emulators and trace solutions for 16-bit and 32-bit microcontrollers. The software architecture of the Universal Debug Engine (UDE) guarantees optimal conditions for debugging SoC-based systems. For example, by means of the intelligent use of modern on-chip debugging and on-chip trace units, valuable functions such as profiling and code coverage are available for the system optimization. Furthermore, the associated Universal Access Device (UAD2/UAD3+) product family, with transfer rates of up to 3.5 MBytes/s and a wide range of interfaces, offers entirely new dimensions for fast and flexible access to multi-core systems. Important architectures such as TriCore, Power Architecture, XC2000/XE166, ARM, Cortex, SH-2A, XScale and C166/ST10 as well as simulation platforms of different vendors are supported. For further information about the company, please visit www.pls mc.com.

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