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Simplifies development with complex heterogeneous high-end SoCs:

PLS' UDE 4.6 once again sets new standards in the areas of trace functions, multicore debugging and test automation

Lauta (Germany) – January 12, 2016 – PLS Programmierbare Logik & Systeme has not only expanded the latest version of its Universal Debug Engine (UDE) with a number of additional trace and debugging functions, but has also added completely new features for test automation. This now enables users to utilize the enormous performance of the newest multicore System-on-Chip (SoC) families, with as few restrictions as possible. The UDE 4.6, which PLS is presenting for the first time at embedded world 2016 in Hall 4, Booth 310, supports a wide range of different architectures and new device families such as: the Power Architecture-based SPC58 E series and the ARM Cortex-M7 core-based STM32F7 series from STMicroelectronics, the XMC4800 devices from Infineon, which are the first-ever ARM Cortex-M4-based microcontrollers with EtherCAT integrated, and the Zynq-7000 family from Xilinx, which is equipped with a dual-core ARM Cortex-A9 and additional FPGA.

The Universal Emulation Configurator (UEC) of the UDE for definition of trace-based measurement tasks has been expanded with a library for the Mini-MCDS (Multi-Core Debug Solution) of the current AURIX devices from Infineon. This means that some of the diagnostic possibilities, which until now were only offered by special Emulation Devices, are now available for the first time in production chips. A JTAG standard debug interface or Debug Access Port (DAP) on the target is the only requirement for the use of this feature.

Another significant innovation: With the UDE 4.6, support for Synopsys' Virtualizer simulator platform has been expanded to multicore systems. Therefore, the UDE can also be used as a frontend for multicore simulations based on AUIRX/TriCore, Power Architecture or ARM core models.

Furthermore, thanks to the innovative approach of persistent trace streams within the UDE, export of trace data as well as their subsequent import and an offline analysis without a cost-intensive Hardware-in-the-Loop (HiL) target environment is also now possible. Management of the various trace recordings with freely selectable designations and exact timestamps takes place directly in the debugger's user interface.

Smart filter functions for the symbol and peripheral register selection simplify the navigation even in large applications and very complex SoCs.

The Microsoft Component Object Model (COM)-based software interface of the UDE also presents itself even more convenient and powerful than before. For example, the possibilities for loading multicore applications as well as setting breakpoints by third-party tools have been significantly enhanced and simplified. Additional completely new functions now allow automatic configuration, execution and documentation of code coverage measurements both by own macros and also by external tools. This effectively supports the creation of test workflows for ensuring the software quality in compliance with ISO 26262.

The complete cross-debugger functionality of the UDE 4.6 is also available as an own debug perspective also within the Eclipse environment including the current Eclipse version 4.5 (Mars) and CDT 8.7.

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PLS Programmierbare Logik & Systeme GmbH

PLS Programierbare Logik & Systeme GmbH, based in Lauta, Germany, was founded in 1990. With its innovative modular test and development tools, the company has been one of the international technology leaders in the field of debuggers, emulators and trace solutions for 16-bit and 32-bit microcontrollers for over two decades. The software architecture of the Universal Debug Engine (UDE) guarantees optimal conditions for debugging SoC-based systems. For example, by means of the intelligent use of modern on-chip debugging and on-chip trace units, valuable functions such as profiling and code coverage are available for the system optimization. Furthermore, the associated Universal Access Device (UAD2/UAD3+) product family, with transfer rates of up to 3.5 Mbytes/s and a wide range of interfaces, offers entirely new dimensions for fast and flexible access to multicore systems. Important architectures such as AURIX/TriCore, Power Architecture, Cortex/ARM, XC2000/XE166 as well as simulation platforms of different vendors are supported. For further information about the company, please visit www.pls mc.com.

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